SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

Digital Power Factor Correction with Non-Sinewave Current

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INTRODUCTION

Since the European and International standards limit current harmonics content, Power Factor is becoming an important feature for mains supplied equipment.
Power Factor is defined by the ratio of the Real Power to the Total Apparent Power.(cf. ref. [2] page 14).

$$\text{P.F.} = \frac{P}{S} = \frac{\text{REAL POWER}}{\text{TOTAL APPARENT POWER}}$$

The theoretical calculation for a non-ideal sinusoidal signal gives the final definition of Power Factor

$$\text{P.F.} = \cos\theta.\cos\varphi$$

in which φ is the displacement angle between the input voltage and the in-phase fundamental current signal and $\cos\varphi$ is the coefficient characterizing the waveform distortion. This coefficient is linked to the current harmonic content and is affected by the IEC555 standard.

Today, several applications already use Power Factor Corrector (P.F.C.) dedicated IC's.
This note describes an original P.F.C. technique using a standard microcontroller which meet the emerging standards.

The digital technique illustrated here, allow the current waveform drawn from the mains to be synthesised and to adapt its amplitude to particular requirements.

In our example, we built a voltage pre-regulator using boost topology to generate 400V DC voltage. This DC voltage is regulated by an ST9 microcontroller. The microcontroller also manages the harmonic reduction and other safety features.

1 PRINCIPLE

In most equipment supplied from the mains, the first step is to rectify the sine wave and to charge the bulk capacitor to get the DC voltage.
As shown in Figure 1, the current drawn from the mains is pulsed at each peak of the line voltage. This pulsed current generates multiple harmonic currents and gives a poor power factor (typically between 0.5 and 0.7). This Power Factor does not comply with the permissible amplitudes of the various harmonic constituents defined by the present or future standard (EN6055, IEC555). The IEC555 limits are low and generally need special harmonic correction circuits.
One simple solution to put the harmonic levels under the standard limits is to draw from the mains a non-sinewave current, not so sharp, and wider, as shown in the Figure 2.

Figure 1. Full Wave Bridge Rectifier Generates Pulsed Current Inducing Multiple Harmonic Currents And Gives

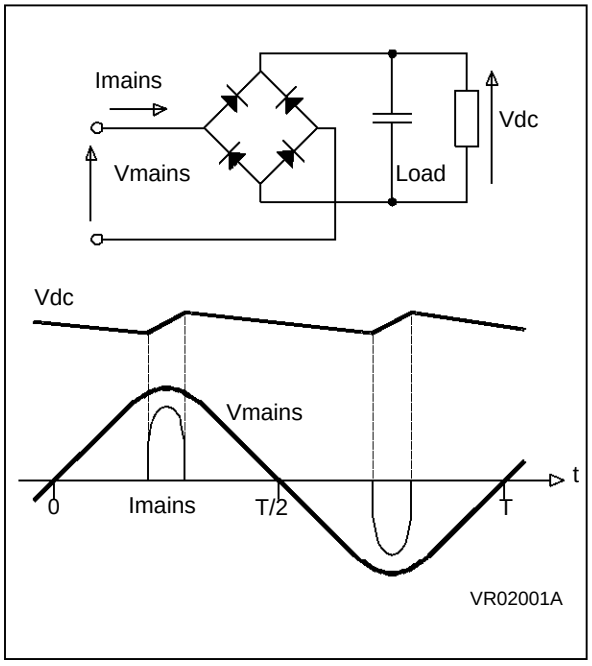
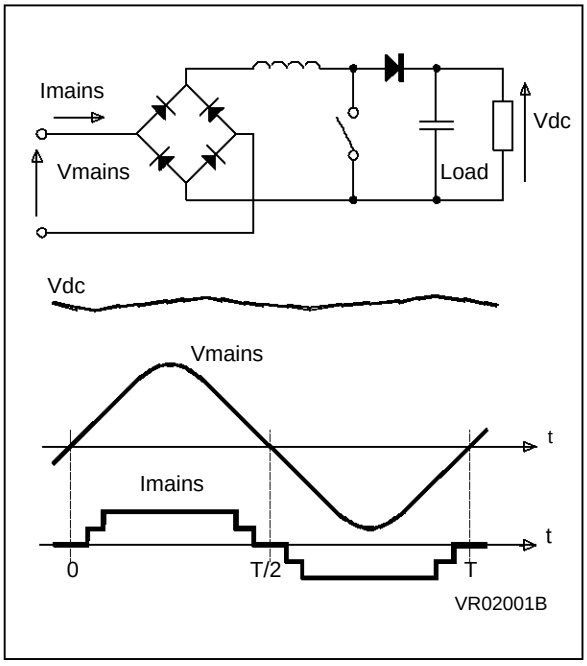


Figure 2. Pre-Regulator Power Factor Corrector Drawing From The Mains A Non-Sinewave Current.



On Figure 3a the input current takes the values 0 and $I_L/2$ at the beginning and at the end of each half period (ie: when the mains voltage is nil or very low) and takes a DC value in-between.
Such a current waveform maximizes the form factor value and the useful power available from a given mains supply.
The shape of this current contains harmonics, each of which must remain under the acceptable limits fixed by the standards. An other way is to calculate by the Fourier transformation the corresponding current maximum value of I_L (Figure. 3a) available from the mains and keep each harmonic under the permissible value. The calculation is given in appendix 1, the results are summarized in Figure 3b.

One simple current waveform (Figure. 3a) gives an harmonic repartition in which the harmonics 19 and 21 mainly limit (Figure. 3b) the maximum permissible current value of the line current I_L to 2.8 A. With this value, the 50 Hz fundamental current is 2.18 A_{RMS} corresponding to an input power of 500 Watts.

Figure 3A. Mains Current Waveform Giving A Fundamental Current Of 2.18 A_{rms} Corresponding To An Input Power Of 500 Watts.

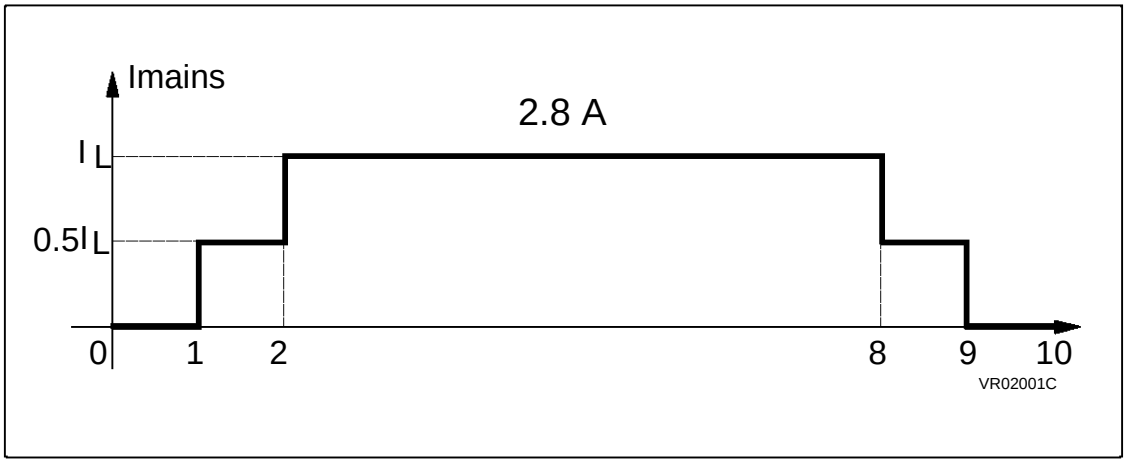
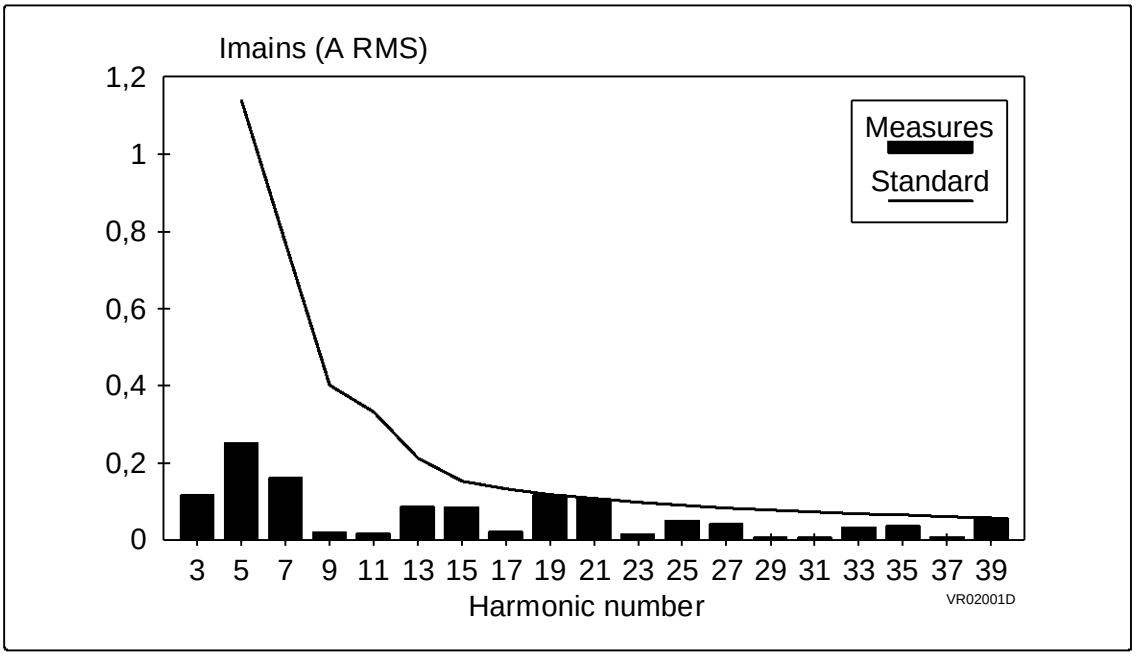


Figure 3B. With The Mains Current Waveform Shown In Figure 3A, The Harmonics 19 And 21 Limit The Available Power To 500 Watts.



Optimizing the current waveform allows the input power available from the mains to be increased. By slightly changing the instant of the rising and the falling edge of the current (Figure 3c), the current harmonic repartition is changed: the amplitude of harmonics 19 and 21 are reduced, while the other harmonics amplitudes are slightly increased (Figure.3d)

A 5A line current can now be drawn from the mains given a 4.3 A_{RMS} as fundamental current corresponding to an input power of 1000 Watts.

Figure 3C. Slight Change Of The Current Rising And Falling Edge Instant Allows The Drawing Of 4.3 A_{rms} Fundamental Current Corresponding To An Input Power Of 1000 Watts.

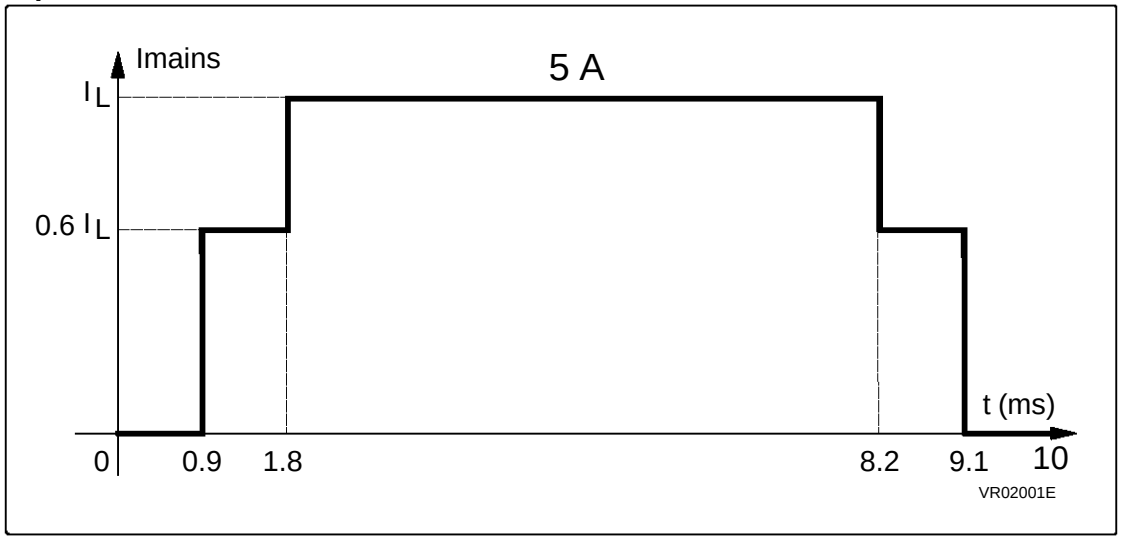
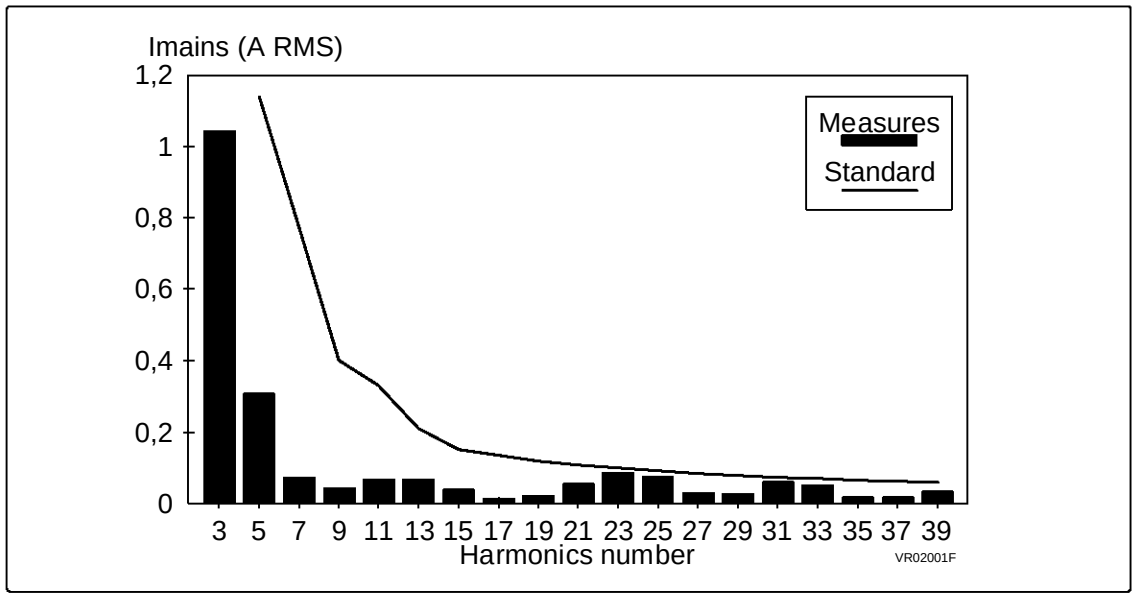


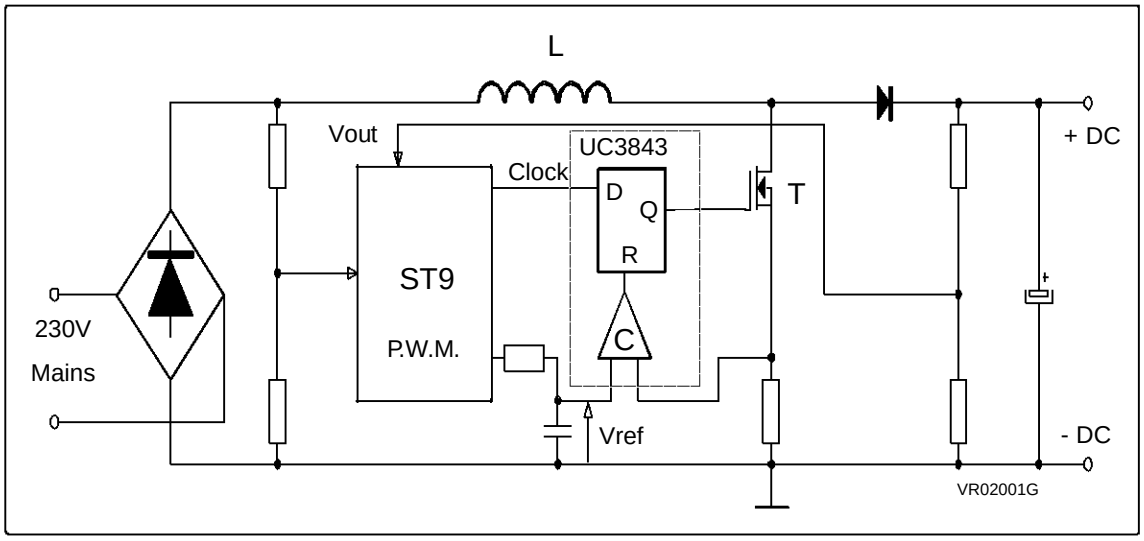
Figure 3D. Optimizing Current Waveform As Shown On Figure 3C Changes The Harmonics Repartition And Increases The Available Input Power Up To 1000



2 PRACTICAL APPLICATION

Figure 4 gives the topology of the power factor pre-regulator arranged in Boost converter configuration and controlled by an ST9 microcontroller.

Figure 4. Digital P.F.C. Block Diagram With St9 Microcontroller And Uc3843 Current Mode P.W.M. Control Ic.



This circuitry aims to deliver the power requested by the output load under a regulated voltage and to draw from the mains a non-sinusoidal current as shown in Figure 3a.
Control of the mains current waveform and regulation of the output voltage require two dependant closed loops.

2.1 DC output voltage regulation loop

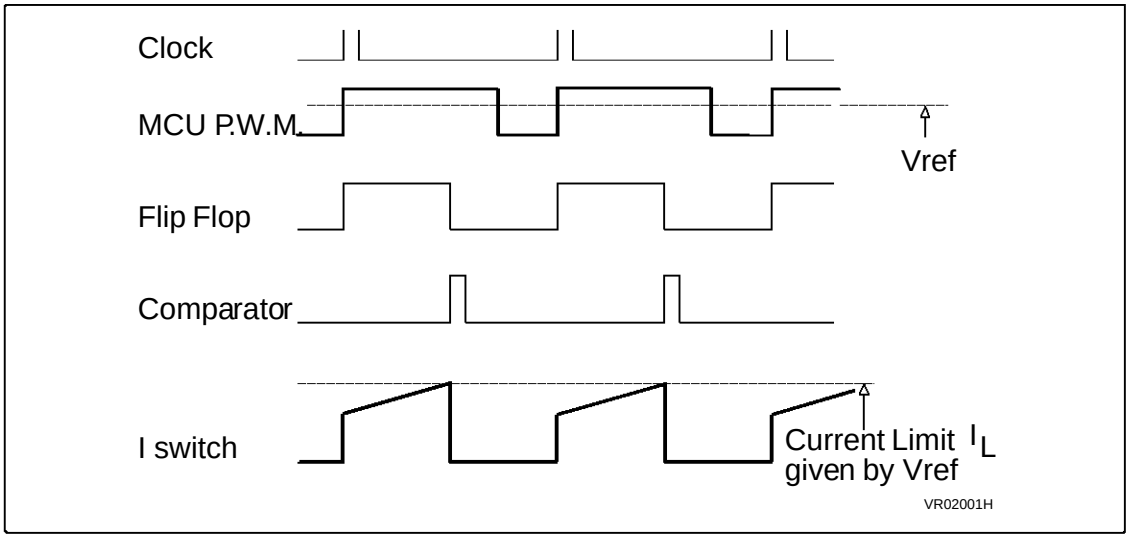
When the load is varying, the output voltage is kept constant by the DC output voltage regulation loop (which is a slow loop response as detailed in paragraph 3).
In order to do this, the output voltage is measured through a resistor bridge and one of the microcontroller A/D converter channels. A setpoint for the current regulation loop is calculated with the output DC voltage variations. This setpoint is provided by one of the microcontroller internal timer in P.W.M. mode. This gives a voltage reference V_{ref} after filtering as shown in Figure 4.

2.2 Current regulation loop

The current regulation loop controlling the current waveform is based on a comparator, a flip-flop and a power transistor. (This loop is fast because the current in the switch reacts at the P.W.M. frequency).
The filtered P.W.M. voltage reference V_{ref}, given by the output voltage regulation loop, is compared to the current sense voltage and defines the peak current value I_L in the power chopper transistor.

The P.W.M. current in the power transistor is synchronized by a clock from the microcontroller (Figure. 5). On the rising edge of the clock, the flip-flop is set, the power transistor turns ON, and the current increases in the inductor. When the current reaches the limit I_L given by V_{ref}, the flip-flop is reset by the comparator and the power transistor turns OFF. In the practice, we use a UC3843 current mode P.W.M. control IC including one comparator, one flip-flop and a 15 Volt buffer able to directly drive the power MOS.

Figure 5. Current Regulation Loop Timing: The Switch Current Is Turned On By The Clock And Turned Off When Reaching I_l Defined By V_{ref}.



2.3 Shaping mains current waveform

In order to obtain the current outline shown in Figure 3a, the I_L value is computed at the beginning of each half cycle according to the corrections asked by the output DC voltage regulation loop. The current waveform is synchronized upon the mains voltage zero crossing. This zero crossing detection is made using one of the microcontroller A/D converter channels (cf paragraph 3.3.).

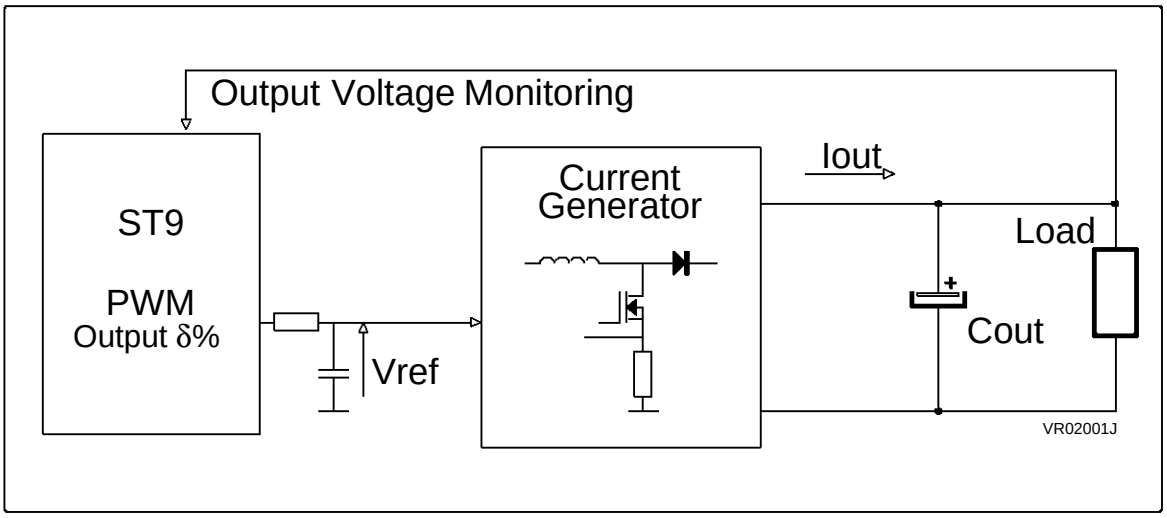
The new duty cycle elaborated after this measurement is applied synchronously with the mains zero crossing. Three coefficients 0%, 50%, 100%, are automatically applied to this P.W.M. value at specific instant of each period (1,2,8,9 ms). This gives the current shape shown on Figure 3a.

Voltage regulation principle

To study the voltage regulation principle, we consider the simplified diagram shown on Figure 6.

The output capacitor value C_{out} is 220 µF. The power varies from 0 to 400 Watts under a fixed output voltage of 400 V. The current generator supplying the output current I_{out} is a boost stage regulated in current mode. The reference voltage V_{ref} results from the filtered P.W.M. duty cycle generated by the microcontroller multifunction Timer.

Figure 6. Principle Of A Pre-Regulator, Controlled By A Microcontroller, Supplying A Load With A Regulated Voltage.



The voltage regulation loop, keeping the output voltage constant when the load varies is characterized by the transfer function of the current generator. It is obtained by measuring in open loop the global relation between the duty cycle variation $\Delta\delta$ and the output current variation ΔI_{out}.

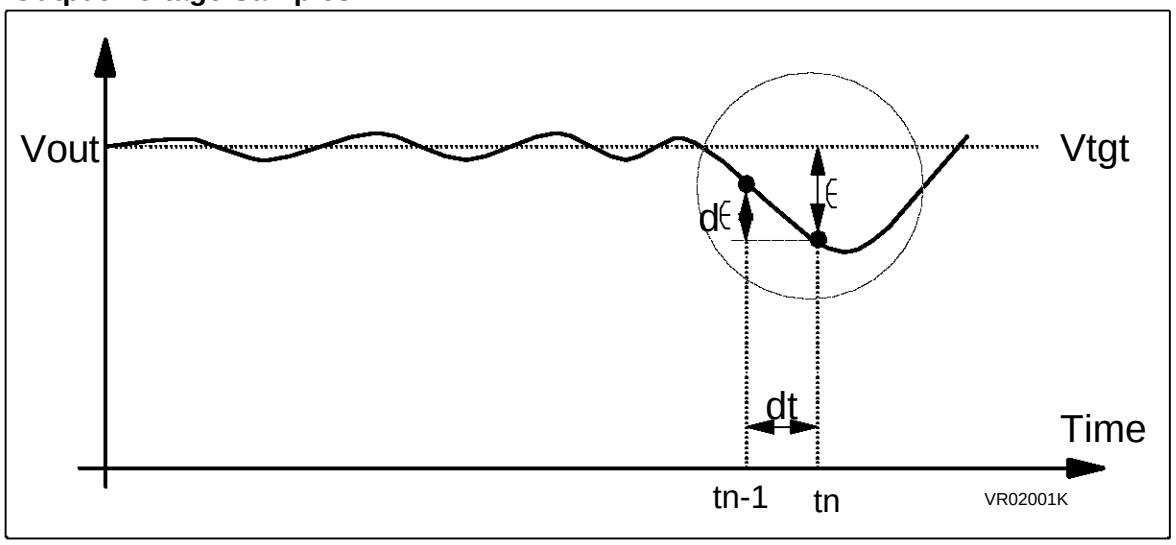
$$\Delta\delta_{(\%)} = 50 \times \Delta I_{out(A)} \quad \text{with} \quad \begin{matrix} V_{line} = 220V \\ C = 220\mu F \\ V_{out} = 400V \end{matrix} \qquad (5)$$

The microcontroller takes the output voltage into account once per sine period (9ms after the previous zero crossing) by means of its A/D converter. It computes the difference between this measurement and the output voltage target value (V_{tgt}) stored in its memory and compensates the detected error (ε) by modifying ($\pm \Delta\delta$) the previous PWM duty cycle. The new PWM duty cycle will be:

$$\delta_{\%} = \delta_{n-1(\%)} + \Delta\delta \qquad (6)$$

To complete static and dynamic output voltage regulation, the microcontroller uses two consecutive samples of the output voltage and computes the static error ε and its speed variation dε/dt.(Figure.7).

Figure 7. To Perform The Output Voltage Regulation, The Mcu Calculates The Static Voltage Error E And Its Speed Varation Dε/Dt Using Two Consecutive Output Voltage Samples.



2.4 Static error compensation, S - Static parameter

At each sample of the output voltage, the microcontroller evaluates the voltage error ε_n between the output voltage V_{out} and the targeted voltage V_{tgt} stored in memory:

$$\varepsilon_n = V_{out} - V_{tgt} \qquad @t_n \qquad (7)$$

In order to compensate this error, the microcontroller computes the current change (ΔI_{out}) necessary to complete the capacitor charge during a fixed time (ΔT). The choice of this time value gives the response time of the voltage compensation.

$$\Delta I_{out} = -C \frac{\varepsilon_n}{\Delta T} \qquad (8)$$

Combining equations (5) and (8), we obtain the duty-cycle variation necessary to compensate the voltage error.

$$\Delta\delta_{(\%)} = -50C \frac{\varepsilon_n}{\Delta T} = S \times \varepsilon_n \qquad (9)$$

The static compensation parameter S depends on the output capacitor value and defines the chosen response time (ΔT). This parameter must to be adapted according to the required response time behaviour for each particular application. It is stored in the microcontroller memory.

In our application: C = 220µF, and ΔT = 50ms (response time 5 times longer than the sample period), we get the relation:

$$\Delta\delta_{(\%)} = -50 \frac{220\ 10^{-6}}{50\ 10^{-3}} \varepsilon_n = -0.2\ \varepsilon_n \qquad \textbf{(10)}$$

Example: if detecting 10 Volts under-voltage, the duty-cycle will be increased by 2%; 50ms later the voltage variation will be completely cancelled.

2.5 Dynamic compensation, D - Dynamic parameter

Between two consecutive samples of output voltage and referring to the previous measurement, the microcontroller computes the speed variation of the error dε/dt:

$$\frac{d\varepsilon}{dt} = \frac{\varepsilon_n - \varepsilon_{n-1}}{t_n - t_{n-1}} \qquad \textbf{(11)}$$

This output voltage speed variation comes from a difference ΔI between the input and the output capacitor current. This is due to a load variation or to mains voltage variation. This current difference is directly given by the voltage variation speed:

$$\Delta I = C \frac{d\varepsilon}{dt} \qquad \textbf{(12)}$$

One strategy to immediately stop the voltage variation is by compensating this current difference with the same opposite quantity. By combining (5) and (12), we obtain the corresponding change of δ.

$$\Delta\delta_{(\%)} = -50\ \Delta I = -50\ C \frac{d\varepsilon}{dt} = D\ x\ d\varepsilon_{(v)} \qquad \textbf{(13)}$$

The dynamic compensation parameter D depends on the output capacitor and the time interval (dt) between two consecutive measurements. This parameter has to be adapted to the particular application and then stored in the microcontroller memory.

In our application: when C = 220µF and dt = 10ms between two voltage measurements, we get:

$$\Delta\delta = -1\ x\ d\varepsilon \qquad \textbf{(14)}$$

Example: if detecting 50V between two successive measurements, the duty-cycle has to be increased by 50% to immediately stop this voltage variation speed.

The global relationship giving the duty-cycle change after each voltage measurement is given by the relation (15). This cancels the voltage variation speed and compensates the error voltage in 50ms. The S and D parameters are the regulation loop parameters, which required to be adapted to each application and to be stored in microcontroller memory.

$$\Delta\delta = (S.\varepsilon) + (D.d\varepsilon) \qquad S = -\frac{50\ C}{\Delta t} \qquad D = -\frac{50\ C}{dt} \tag{15}$$

With the numerical parameters, in our application, we obtain:

$$\Delta\delta_{(\%)} = -0.2\ \varepsilon(v) - 1\ d\varepsilon_{(v)} \tag{16}$$

2.6 Voltage measurement and zero crossing procedure

To avoid wrong voltage measurement and to obtain good electrical immunity, a digital filter is implemented by software. This filter is made by making the average of three output voltage measurements. Each measurement is separated in time by 100µs.

In order to synchronize the current waveform to the mains voltage, zero crossing detection is performed by the software. The mains voltage is sensed every one millisecond. Before the end of the period (9ms after the previous zero crossing), the A/D converter mode is changed to a continuous conversion mode. When the output voltage goes through 50V a zero crossing signal is generated after a 0.5ms delay. A restart of the time base is done. Without zero crossing detection, synchronization is performed by default by the current time base timer.

2.7 Safety functions

Software security functions can be easily implemented due to the periodic output voltage measurement. This measurement is automatically performed every millisecond through the microcontroller A/D converter. The main security is the output over-voltage detection. It stops the P.F.C. when the output voltage reaches 450V. The system starts again with a P.W.M. duty cycle equal to zero when the output voltage decreases under 420V. This security prevents from dangerous over-voltages caused by an open load commutation.

By using other A/D converter channels, several other securities have been implemented by software:

- voltage monitoring on Power switch gates (the system can be stopped when the gate voltage decreases under a fixed value: eg 13V).
- at power on, the P.F.C. function only starts if the output voltage is greater than a predefined value.
- mains voltage monitoring: the system stops if mains voltage is too low.
- short circuit detection. A serial switch is often required to open the circuit and disconnect the load. The management of this serial switch can be made by the microcontroller providing also a soft start.

Practical Results
A 400V DC pre-regulator including harmonic correction controlled by the SGS-THOMSON ST9 microcontroller is shown on appendix 2. The implementation of the Power Factor Correction within the ST9 requires one multifunction timer (for PWM generation) and three channels of the A/D converter (for voltage monitoring). Several other peripherals functions of the ST9 remain free for the user:

- one MultiFunction Timer,
- 4 A/D Converter channels,
- one Serial Communication Interface (SCI),
- one Serial Peripheral Interface (SPI),
- one WatchDog Timer
- Direct Memory Access controller

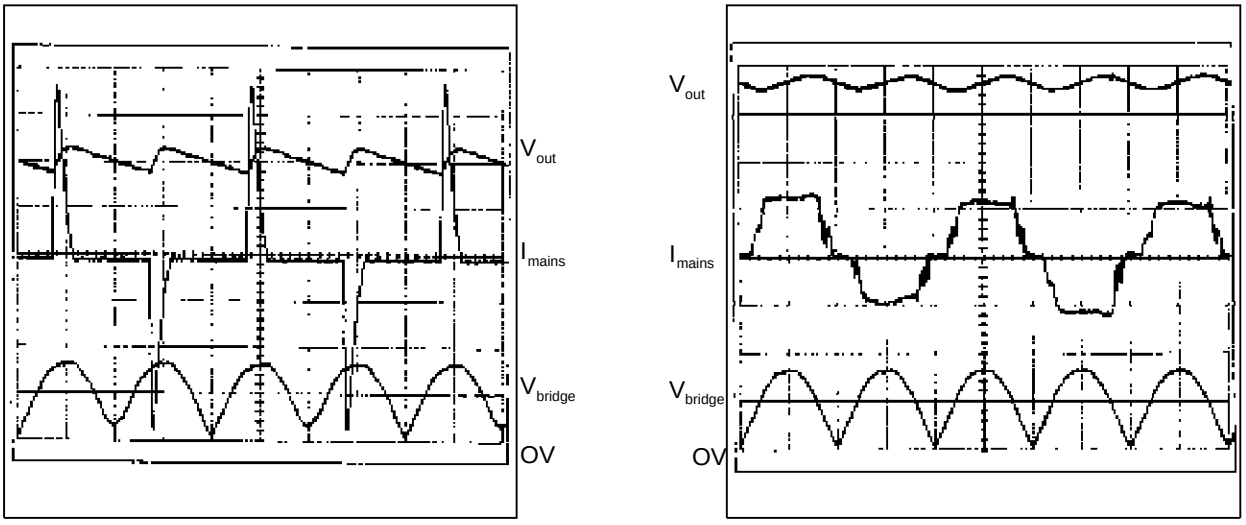
Consequently, the ST9 microcontroller is able to manage both of P.F.C. pre-regulator and a downstream converter application such as 3-phase Induction Motor Drive (cf. ref. [4] page 14, U.P.S., and also the associated bus management.

To evaluate the performances of this digital Power Factor Corrector, two main tests have been performed.

2.8 Static response

In this case, the P.F.C. is permanently loaded with a 400W resistive load.
Figure 8 compares the current waveshape in the mains obtained with and without Power Factor Correction.

Figure 8. Comparison Of The Current Waveshape In The Mains Obtained With Or Without Digital P.F.C.



A) Without P.F.C.

B) With P.F.C.

Load = 400W; 5Ms/• ; V_{out}:50V/• ; V_{Bridge}:200V/• ; I_{mains}:2A/•

When the digital P.F.C. is used:

- The mains current is in phase with the mains voltage
- The output voltage ripple is reduced to 15V peak to peak
- the peak current is limited to 2.2 A instead of 7A peak.

Furthermore, we tested the DC voltage regulation loop to keep a output DC voltage of 400V supply a 400W load when the mains voltage varies from 140V to 300V. The output DC voltage variations remains under 2%.

The harmonic measurements on the mains current made by a Fast Fourier Transform, for a 400W output power are summarized in the following table (Table 1).

Table 1. Harmonic Current Repartition Using Or Not A Digital P.F.C. And Compared To

	I_{mains} Load = 400W	Harmonic order # n				
		1	2	3	4	5
I_{rms}(A) with P.F.C.	1,80	1,70	0,07	0,25	0	0
I_{rms}(A) without P.F.C.	3	2	1	1	1	0
Standard Limits	-	-	2	1	1	0

By comparing the measurements without P.F.C. it can be check that the two fundamental currents have the same magnitude in both cases. When the P.F.C. is ON, the fundamental current and the mains current have the same order of magnitude and the other current harmonics are drastically reduced.

Global Power Factor can be calculated from current values shown in table below. The phase angle between the input voltage and the mainsfundamental current being very close to 0° ($\cos\varphi = 0.99$), the global power factor is given by the waveform distortion coefficient: (cf. ref. [2] page 14)

$$\frac{\text{I fundamental Term}}{\text{I mains}} = \cos\theta$$

Numerical calculation gives the global power factor value.

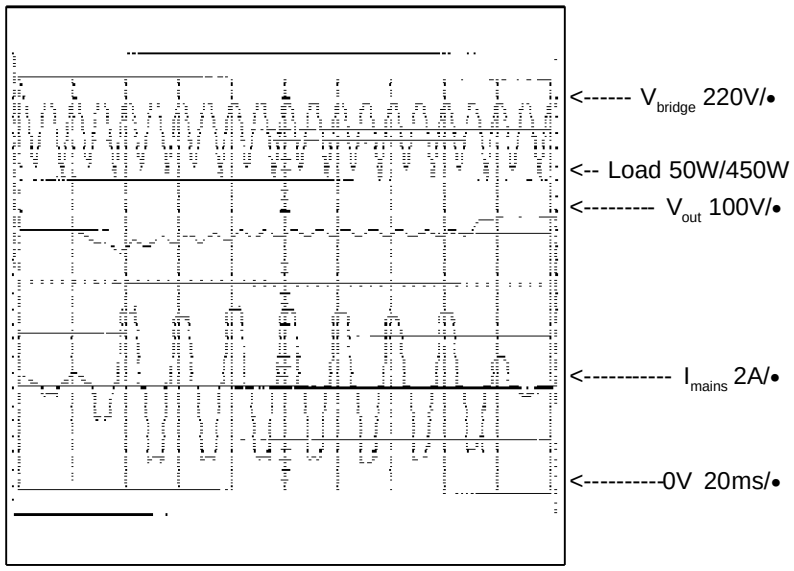
Cosφ with P.F.C.	1
Cosφ without P.F.C.	1

Despite the nonsine waveform of the current drawn from the mains, the global power factor is very close to 1.

2.9 Dynamic response

Figure 9 shows the dynamic response of this digital P.F.C. when the load varies from 50W to 450W. For this load variation, the maximal transient output voltage drop is 40V and the voltage recovers its regulated value within 100ms. For applications requiring faster dynamic response time, this last value can be decreased by reducing the response time (ΔT) as detailed in chapter 3.1. No voltage over-oscillations have been observed.

Figure 9. Dynamic Response Of The Output Voltage Regulation When The Load Is Switched From 50W To 450W.



Conclusion

For application in the power range under one thousand Watts, the Power Factor Correction with the non-sine wave current concept, allows the current harmonic content to stay under the limits fixed by the standard. Moreover, despite the nonsine waveform current drawn from the mains, the global power factor is very close to 1.

The static and dynamic responses are sufficient for many applications and, particularly for the majority of the motor drive used in industrial and home appliances fields.

In applications where a microcontroller is already used, it is easy to implement such a P.F.C controlled and regulated by software. Other features can be implemented such as: fast current loop, voltage regulation, safety functions by voltage monitoring and soft-start procedure.

References

[1] - Circuits for P.F.C with regards to mains filtering by Jean-Marie Bourgeois - ”PCIM - Los Angeles - 1991”

[2]- Understanding Power Factor, Luc Wuidart, Central Application Laboratory, SGS-Thomson microelectronics

[3] - IEC555 standards

[4] - Simplified digital control for three phase induction motor drive, Bruno MAURICE - EPE journal vol 2 Nø 3 October 1992

Appendix 1 : Fourier Harmonics Calculation

All periodical function can be factorized by the Fourier Transform using the following equation:

$$F(t) = a_0 + \sum_{n=1}^{\infty} (a_n \cos n\omega t = b_n \sin n\omega t)$$

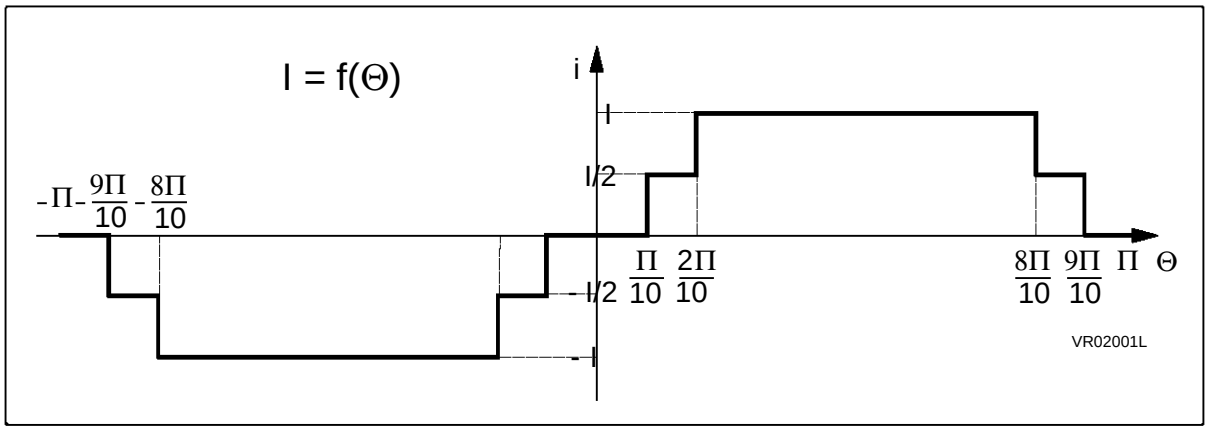
taking: $\theta = \frac{2\pi}{T} t = \omega t$, we get

$$a_{(0)} = \frac{1}{2\pi} \int_{-x}^{x} f_{(\theta)}\, d\theta, \quad a_n = \frac{1}{\pi} \int_{-x}^{x} f_{(\theta)} \cos n\theta\, d\theta, \quad b_n = \frac{1}{\pi} \int_{-x}^{x} f_{(\theta)} \sin n\theta\, d\theta$$

With a shape of current f(θ) equivalent to the one shown on Figure 10, and considering the current is an odd function, a_0 and a_n coefficients are nil and coefficients b_n can be written:

$$b_n = \frac{2}{\pi} \int_{0}^{x} f_{(\theta)} \sin n\theta\, d\theta$$

Figure 10. Shape Of The Current Used For Calculation.



If I is the maximum value of current, bn is given by the following expression:

$$b_n = I \frac{2}{n\pi} [k(\cos n\alpha_1 - \cos n\alpha_2) + \cos n\alpha_2 - \cos n\alpha_3 + k(\cos n\alpha_3 - \cos n\alpha_4)]$$

The expression of the Fourier transform function becomes:

$$F(\theta) = \sum_{n-1}^{\alpha} b_n \sin n\theta$$

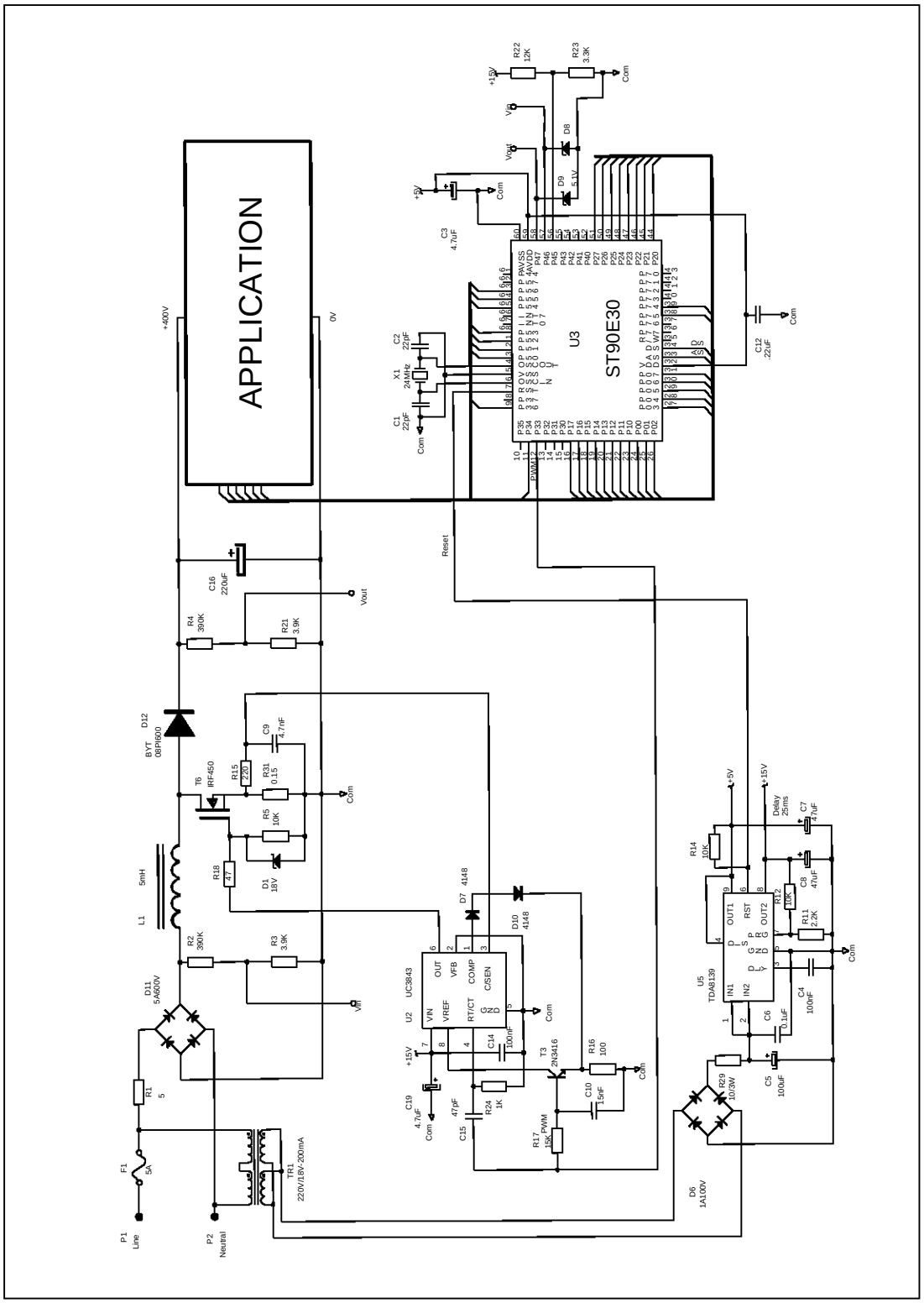
Table 2 shows the calculation for each odd harmonics with:

I=2.8A with k = 0.5 $\alpha_1 = \pi/10$, $\alpha_2 = 2\pi/10$, $\alpha_3 = 8\pi/10$, $\alpha_4 = 9\pi/10$
and with:
I=5A with k = 0.6 $\alpha_1 = 0.9*\pi/10$, $\alpha_2 = 0.8*2\pi/10$, $\alpha_3 = (2-0.8)*8\pi/10$, $\alpha_4 = (2-0.9)*9\pi/10$

The limit of the standard are noted for reference.

Harmonics #	Standard Limits A_{RMS}	Calculated Harmonics (A_{rms})	
		I = 2.8A	I = 5A
1	-	2	4
3	2.3	0.117	1
5	1	0.252	0.309
7	1	0.161	0.074
9	0.4	0	0.044
11	0	0.016	0.068
13	0	0.087	0.069
15	0	0.084	0.039
17	0.132	0.021	0.014
19	0.118	0.117	0.021
21	0.107	0.106	0.055
23	0.098	0.015	0.084
25	0	0	0.076
27	0.083	0.042	0
29	0.073	0.006	0.027
31	0	0.006	0
33	0,068	0.034	0.052
35	0,064	0.036	0.017
37	0,061	0.009	0.018
39	0.058	0.057	0.034

Appendix 2 : Practical schematic
of a digital Power Factor Corrector controlled by a standard ST90E30 microcontroller. Most of its features and the CPU time of the microcontroller remains free, so it can simultaneously control an associated complex application.



NOTES: